CLAIMS

1. A method of replacing a faulty processor element, in a processor array comprising a plurality of processor elements arranged in an array of rows and columns, the processor elements being interconnected by buses running between the rows and columns and by switches located at the intersections of the buses, and the array including a redundant row to which no functionality is initially allocated, the method comprising:

in the event that a first processor element is found to be faulty, removing functionality from the row that contains said first processing element, and allocating functionality to the redundant row.

2. A method as claimed in claim 1, comprising:

allocating the functionality, removed from the row that contains said first processing element, to an adjacent row; and

reallocating the functionality from the adjacent row, to a further row adjacent thereto, as required until functionality has been allocated to the redundant row.

3. A method as claimed in claim 2, wherein the redundant row is located at an edge of the array.

4. A method as claimed in claim 1 or 2, wherein, in operation of said processor array, data is transferred during time slots between processor elements over horizontal buses running between the rows of processor elements and over vertical buses running

between the columns of processor elements, and further comprising:

when allocating functionality to the processor elements, such that data is scheduled to be transferred during a first time slot from a first processor element to a second processor element without using any vertical bus, reserving said time slot for said data transfer on a segment of a vertical bus that would be used in the event of a reallocation of functionality following a determination that either said first processor element or said second processor element were faulty.

5. A method of allocating functionality to a processor array, the processor array comprising a plurality of processor elements arranged in an array of rows and columns, the processor elements being interconnected by buses running between the rows and columns and by switches located at the intersections of the buses, the method comprising:

in the event that a processor element has a fault, allocating no functionality to any processor element in the row containing said processor element.

6. A processor array, comprising:

a plurality of processor elements arranged in an array of rows and columns, wherein the arrangement of processor elements in each row is the same as the arrangements of processor elements in each other row;

pairs of horizontal buses running between the rows of processor elements, each pair comprising a first horizontal bus carrying data in a first direction and a second horizontal bus carrying data in a second direction opposite to the first direction;

vertical buses running between the columns of processor elements, wherein some pairs of adjacent columns of processor elements have no vertical buses running therebetween, and other pairs of adjacent columns have two buses carrying data in a first direction and two buses carrying data in a second direction opposite to the first direction running therebetween; and

switches located at the intersections of the horizontal and vertical buses.

7. A processor array as claimed in claim 6, wherein each switch comprises:

a plurality of input buses and a plurality of output buses;

a memory device, which stores information at each address thereof, indicating what data is to be switched onto each of the output buses; and

a controller, for counting through addresses of the memory device in a predetermined sequence.

8. A processor array as claimed in claim 7, wherein the memory device stores information which indicates whether the data to be switched onto each of the output buses is:

the data value on one of the input buses;

the previous data value on said output bus; or

the value zero.